ANALYSIS AND DESIGN OF DIGITAL INTEGRATED CIRCUITS

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The *device transconductance parameter* is defined as $k = k'(W/L)$. Substituting this in the above yields

$$I_D = \frac{k}{2}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \qquad V_{GS} \geq V_T \qquad (2.11b)$$
$$V_{DS} \leq (V_{GS} - V_T)$$

for the so-called *linear* region of operation. This equation is important. It describes the current-voltage (I-V) characteristics of the MOS transistor assuming a continuous channel is present from source to drain. Typical values of k' for $t_{ox} = 0.1$ μm are about 20 μA/V^2 for NMOS and 8 μA/V^2 for PMOS devices.

As the value of V_{DS} is increased, the induced conducting channel charge Q_I decreases near the drain. Equation (2.9) shows that Q_I at the drain end approaches zero as V_{DS} approaches $V_{GS} - V_T$. When V_{DS} equals or exceeds $V_{GS} - V_T$, the channel is said to be *pinched off*. Increases in V_{DS} above this critical voltage produce little change in I_D, and Eq. (2.11) no longer applies. The value of I_D in this region is obtained by substituting $V_{DS} = V_{GS} - V_T$ in Eq. (2.11*b*), giving

$$I_D = \frac{k}{2}(V_{GS} - V_T)^2 \qquad V_{GS} \geq V_T \qquad (2.12)$$
$$V_{DS} \geq (V_{GS} - V_T)$$

for the MOS transistor operating in this so-called *saturation* region.* The word "saturation" is used because I_D reaches a limit, or saturates, at the level given by Eq. (2.12). The choice of word is unfortunate because the same word has a different meaning in relation to bipolar transistor operation.

The drain current of an MOS transistor in the saturation region in fact is not completely independent of V_{DS}, because the depletion layer at the drain widens as V_{DS} increases, shortening the electrically effective value of L. Also, there is significant electrostatic coupling between the drain and the mobile charge in the channel, such that increasing drain voltage increases Q_I above the value given by Eq. (2.9). Each of these effects acts to increase the drain current as drain voltage increases. An empirical approximation to the actual drain current is given by

$$I_D = \frac{k}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \qquad (2.13)$$

where the *channel-length modulation parameter* λ (lambda) has typical values in the range 0.1 to 0.01 V^{-1} and represents the small influence of V_{DS} on I_D in saturation. To avoid discontinuities in the $I_D - V_{DS}$ characteristic, the

*The consequences of the earlier assumption of V_T constant along the channel may now be understood. In fact, V_T increases with $V(y)$ due to body effect. The result is that saturated drain current I_D is 10 to 40% smaller than the value given by Eq. (2.12). However, good accuracy is obtained in circuit design if the value used for k' is determined from data taken with the transistor operating in saturation.

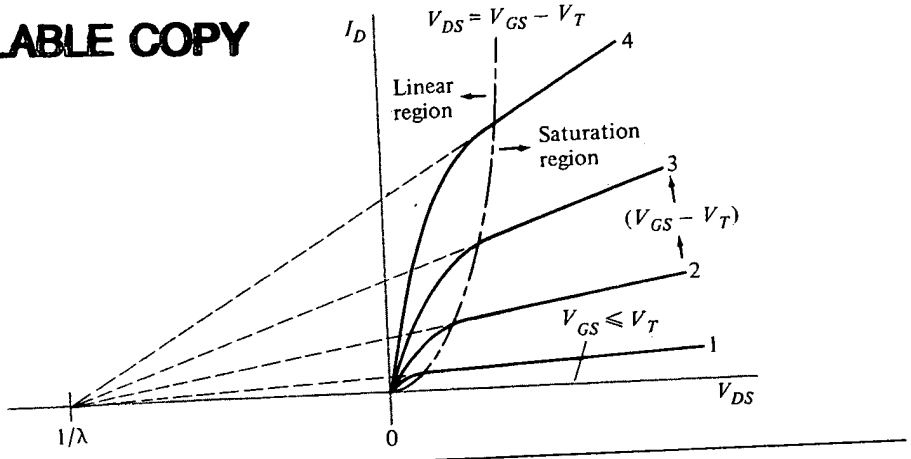

Figure 2.5 NMOS device $I_D - V_{DS}$ characteristics. Channel length modulation parameter here is much smaller than usual, leading to a steeper slope for I_D in saturation than is usually observed.

$(1 + \lambda V_{DS})$ term may be included for both saturated and linear regions with negligible error. Usually the value of λ has little effect on the operating characteristics of digital MOS circuits. Unless otherwise stated, $\lambda = 0$ is assumed in this book.

A plot of I_D versus V_{DS} for an NMOS transistor is shown in Fig. 2.5. Below pinch-off the device behaves as a nonlinear voltage-controlled resistor. This is termed the *linear*, *resistance*, *triode*, or *nonsaturation*, region of operation. Above pinch-off the device approximates a voltage-controlled current source. Note that for depletion-mode NMOS devices, V_T is negative and drain current can flow even for $V_{GS} = 0$. For PMOS devices all polarities of voltages and current are reversed.

As we will see in the next chapter, MOS circuits are usually designed with MOS transistors as the only circuit elements. One or two values of threshold voltage V_T are usually available on a chip. Transistor width W and length L are typically the only parameters available to be specified by the circuit designer.

EXERCISE 2.2

An NMOS transistor with $k = 20\ \mu A/V^2$ and $V_T = 1.5$ V is operated at $V_{GS} = 5$ V and $I_{DS} = 100\ \mu A$. Determine whether Eq. (2.11) or Eq. (2.12) is appropriate, and find V_{DS}.

2.5 CAPACITANCES OF THE MOS TRANSISTOR

Since the MOS transistor is a field-effect device (majority carriers only), the switching speed of MOS digital circuits is limited only by the time required to

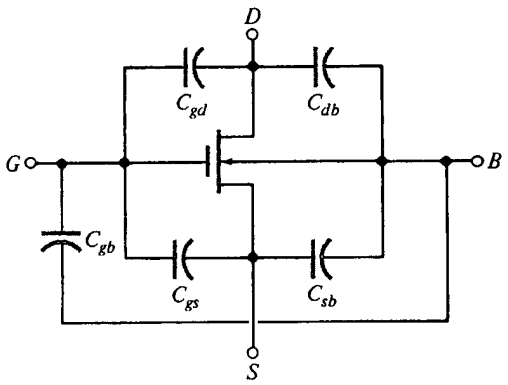

Figure 2.6 MOS transistor capacitances. $C_g = C_{gs} + C_{gb} + C_{gd}$.

charge and discharge the capacitances between device electrodes and from interconnecting lines to ground or other lines. Within LSI circuits all of these capacitances are so small (each in the approximate range 0.01 to 1 pF) that they are difficult or impossible to measure directly. For circuit analysis, these capacitances must be calculated from data on internal device dimensions and dielectric constants.

Figure 2.6 shows the significant capacitances between electrodes of an MOS transistor. The capacitances C_{sb} and C_{db} are n^+p junction capacitances that are readily calculated as shown in Sec. 4.3. For the present, we assume that measured values of junction capacitance are given. Concerning the capacitances from gate to other electrodes, to a first approximation, the sum C_g of C_{gs}, C_{gb}, and C_{gd} is constant, equal to

$$C_g = WLC_{ox} = WL\frac{\epsilon_{ox}}{t_{ox}} \tag{2.14}$$

where C_{ox} is the capacitance per unit area of the gate dielectric as defined in Eq. (2.8).

The division of C_g into its three elements is fairly complex and varies depending on whether the device is in the cutoff, linear, or saturation region. The SPICE circuit analysis program makes the necessary calculations from data on oxide thickness and device dimensions. Further details on modeling of transistor capacitances for hand analysis are presented in Sec. 3.3.2.

Probably the most significant limitation on logic delays and clock rate in LSI digital systems is the capacitances of off-chip connections. Capacitance on an off-chip connection includes device protection (see below), bonding pad, package, and printed wiring board capacitance, and totals 5 to 10 pF per connection on each chip. One LSI circuit may have to drive a number of others, so total capacitance which must be driven can reach 100 pF or more.

The above comments relate to limits on the maximum operating speed of MOS transistor circuits. There is an important limitation on the minimum

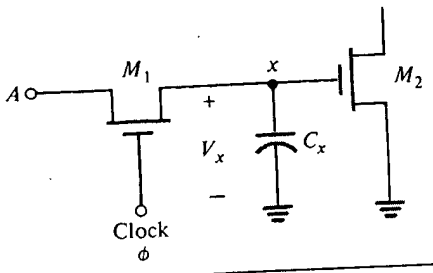

Figure 2.7 Essentials of dynamic MOS circuit operation. C_x is the total capacitance at node X.

operating speed of certain MOS logic and memory circuits known as *dynamic* circuits. For proper operation, these circuits rely upon storage of logic information as charge on the small capacitance of a circuit node, as illustrated in Fig. 2.7.

The circuit of Fig. 2.7 operates as follows. With a logic 1 or 0 on node A, M_1 is turned on, then turned off, by clock signal ϕ. While M_1 is on, the high or low voltage at A is transferred to node x, charging the node capacitance C_x. If a logic 1 is present, M_2 is supposed to retain a conducting channel after M_1 turns off due to the high voltage stored on C_x. However, the charge on C_x leaks away through the n^+p junction of M_1. The rate of leakage determines how long the desired logic signal will be safely represented by V_x, and thus the maximum allowable repetition period for clock signal ϕ. A typical value for C_x is 0.1 pF; increasing this is not desirable because it would consume additional chip area. The reverse (or leakage) current for an n^+p junction in an MOS circuit at maximum temperature might range as high as 1 to 10 pA. This leads to leakage rates in the range 0.01 to 0.1 V/ms. A common specification for minimum clock rate for such circuits is 500 Hz, corresponding to a 2-ms clock period.

EXERCISE 2.3

Calculate approximate values of C_g, C_{sb}, and C_{db} for a silicon-gate MOS transistor for which

$L = 5\ \mu m$ $\quad W = 20\ \mu m$

Source, drain surface dimensions $= 6 \times 24\ \mu m$

Source, drain doping $= 10^{20}/cm^3$

Body doping $= 5 \times 10^{14}/cm^2$

$t_{ox} = 700$ Å

EXERCISE 2.4

Calculate the capacitance of a conducting line 0.5 cm long and 6 μm wide. It is separated from the body by 5000 Å of silicon dioxide. Compare this with the device capacitances calculated in Exercise 2.3.

EXERCISE 2.5

Calculate the average current $I_{(av)}$ needed to drive a 100-pF load through a 2-V change in 30 ns. (MOS transistors with very large W/L ratios are needed to drive such off-chip connections with acceptably small delays.)

2.6 MODELING THE MOS TRANSISTOR FOR CIRCUIT SIMULATION

Computer circuit simulators are essential tools in the analysis and design of MOSLSI circuits. Computer program SPICE is widely used for such work, and is the basis for examples in this text. Other circuit simulators require similar modeling considerations.

2.6.1 SPICE MOSFET Models

SPICE provides three MOSFET device models which differ in the formulation of the I-V characteristic. Only the LEVEL 1 model, which is the simplest, is considered in this book. The LEVEL 1 model employs exactly the dc equations derived in Secs. 2.3 and 2.4. Simulation accuracy using LEVEL 1 is adequate for most MOS digital circuit analysis and design, provided experimentally determined dc parameters are used.

The dc characteristics of the MOSFET are defined by the device electrical parameters VTO, KP, LAMBDA, PHI, and GAMMA. (Correspondences between SPICE parameter names, which are restricted to use of the uppercase English alphabet, and the algebraic symbols used in the preceding pages are shown in Table 2.2.) Electrical parameters are computed by SPICE if process parameters (NSUB, TOX, ...) are given, but user-specified values always override. VTO is positive (negative) for enhancement-mode and negative (positive) for depletion-mode n-channel (p-channel) devices.

Charge storage is modeled in several parts, defined so they may be calculated easily from actual circuit layouts. Three constant capacitors, CGSO, CGDO, and CGBO, represent gate-source, gate-drain, and gate-body overlap capacitances. The nonlinear gate-channel thin-oxide capacitance is calculated by the program as a function of applied voltages and distributed among the gate, source, drain, and body regions. The sum of all the above-mentioned capacitances is approximately equal to C_g of Sec. 2.5. The nonlinear depletion-layer capacitances, for both source-body and drain-body pn junctions, is divided into bottom and periphery, which vary as the MJ and MJSW power of junction voltage, respectively. These capacitances are determined by the parameters CBD, CBS, CJ, CJSW, MJ, MJSW, and PB.

There are two built-in models of the charge storage effects associated with the thin oxide. LEVEL 1 uses the piecewise-linear voltage-dependent capacitance model proposed by Meyer.* The thin-oxide charge storage effects are included only if TOX is specified in the input description.

*J. E. Meyer, "MOS Models and Circuit Simulation," *RCA Review*, vol. 32 (March 1971), pp. 42–63.

TABLE 2.2.
SPICE MOS TRANSISTOR MODEL PARAMETERS

Symbol	Name	Parameter	Units	Default	Example
	LEVEL	Model index		1	
V_{T0}	VTO	Zero-bias threshold voltage	V	0.0	1.0
k'	KP	Transconductance parameter	A/V^2	2.0E-5	3.1E-5
γ	GAMMA	Bulk threshold parameter	$V^{1/2}$	0.0	0.37
$2\lvert\phi_F\rvert$	PHI	Surface potential	V	0.6	0.65
λ	LAMBDA	Channel-length modulation	1/V	0.0	0.02
r_d	RD	Drain ohmic resistance	Ω	0.0	1.0
r_s	RS	Source ohmic resistance	Ω	0.0	1.0
C_{bd}	CBD	Zero-bias B-D junction capacitance	F	0.0	2.0E-14
C_{bs}	CBS	Zero-bias B-S junction capacitance	F	0.0	2.0E-14
I_s	IS	Bulk junction saturation current	A	1.0E-14	1.0E-15
ϕ_0	PB	Bulk junction potential	V	0.8	0.87
	CGSO	Gate-source overlap capacitance per meter channel width	F/m	0.0	4.0E-11
	CGDO	Gate-drain overlap capacitance per meter channel width	F/m	0.0	4.0E-11
	CGBO	Gate-bulk overlap capacitance per meter channel length	F/m	0.0	2.0E-10
	RSH	Drain and source diffusion sheet resistance	Ω/square	0.0	10.0
C_{j0}	CJ	Zero-bias bulk junction bottom capacitance per square meter of junction area	F/m^2	0.0	2.0E-4
m	MJ	Bulk junction bottom grading coefficient		0.5	0.5
	CJSW	Zero-bias bulk junction sidewall capacitance per meter of junction perimeter	F/m	0.0	1.0E-9
m	MJSW	Bulk junction sidewall grading coefficient		0.33	
	JS	Bulk junction saturation current per square meter of junction area	A/m^2		1.0E-8
t_{ox}	TOX	Oxide thickness	m	1.0E-7	1.0E-7
N_A or N_D	NSUB	Substrate doping	$1/cm^3$	0.0	4.0E15
Q_{ss}/q	NSS	Surface state density	$1/cm^2$	0.0	1.0E10
	NFS	Fast surface state density	$1/cm^2$	0.0	1.0E10
	TPG	Type of gate material: +1 opposite to substrate −1 same as substrate 0 Al gate		1.0	
X_j	XJ	Metallurgical junction depth	m	0.0	1.0E-6
L_D	LD	Lateral diffusion	m	0.0	0.8E-6
μ	UO	Surface mobility	$cm^2/V \cdot s$	600	700

There is some overlap among the parameters describing the junctions; for example, the reverse current can be input either as IS (in A) or as JS (in A/m^2). Whereas the first is an absolute value, the second is multiplied by AD and AS to give the reverse current of the drain and source junctions, respectively. This flexibility has been provided so that junction characteristics can be either entered as absolute values on MODEL cards or related to areas AD and AS

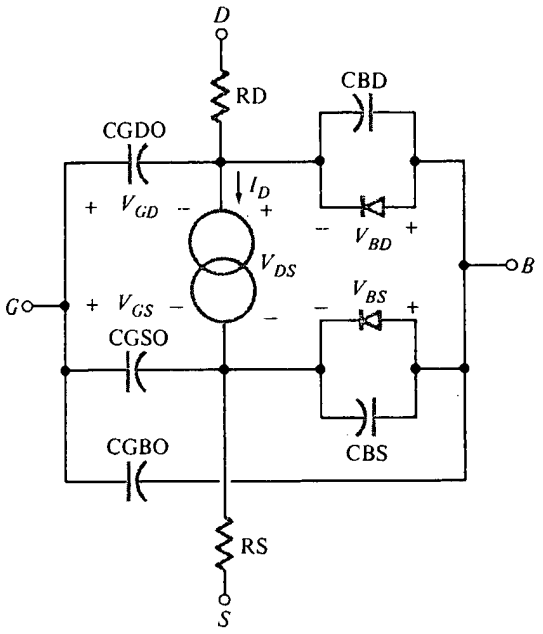

Figure 2.8 SPICE NMOS model, LEVEL I. Drain current I_D as a function of voltages is given by Eqs. (2.6), (2.11), and (2.12). The three gate capacitances shown above represent only the gate overlap outside the active channel region. SPICE calculates the voltage-dependent channel region gate capacitance and allocates it among source, body, and drain.

entered on device cards. The same flexibility is available also for the zero-bias junction capacitances CBD and CBS (in F) on the one hand and CJ (in F/m^2) on the other. The parasitic drain and source series resistance can be expressed as either RD and RS (in Ω) or RSH (in Ω/square), the latter being multiplied by the number of squares NRD and NRS input on the device card.

The SPICE parameters used in LEVEL 1 are listed in Table 2.2 together with the corresponding symbols used in this text. The SPICE MOSFET model is schematically summarized in Fig. 2.8.

Over the past 20 years much effort has gone into analysis of the MOS transistor. Analytical equations much more sophisticated than those presented in Secs. 2.3 and 2.4 have been developed, and more sophisticated models are available as LEVEL 2 and 3 models in SPICE. Nevertheless, it is still impossible to accurately predict transistor current-voltage (I-V) characteristics based only on knowledge of device dimensions and the bulk properties of silicon and silicon dioxide.

To obtain satisfactory results in circuit analysis and design, measured data on samples of MOS transistors must be obtained. Satisfactory results will be obtained for most digital circuits by fitting measured data to Eqs. (2.6),